YNU 横浜国立大学 YOKOHAMA National University

Institute of Advanced Sciences Yokohama National University

IAS-YNU Seminar
先端科学高等研究院

16th Seminar of Research Unit for Extremely Energy-Efficient Processors
超省エネルギープロセッサ研究ユニット
第16回セミナー

Date: 13:30 – 17:00, September 12 (Tuesday), 2017

日程: 平成29年9月12日（火）13:30～17:00

Place: Electrical and Computer Eng. Bldg. 4F, (Seminar room Ⅱ).
場所: 電子情報工学科棟４階（演習室Ⅱ）

【Program】
13:30 – 15:00
N. Yoshikawa, “Overview of research activities in research unit for extremely energy-efficient processors”
T. Ortlepp, “Sensitivity of the AQFP comparator”
J. Stark, “Datacenter computers”
Y. Yamanashi, “Circuit simulation of superconducting circuits containing pi-Josephson junctions by modified JSIM”
N. Takeuchi, “Demonstration of an SSPD using AQFP logic”
C. Ayala, “Progress on AQFP microarchitecture and EDA tools”
Q. Xu, “Recent progress on auto-design-flow-based implementations of AQFP LSI designs”

15:20 – 17:00
F. China, "Demonstration of voltage driver circuit for adiabatic quantum-flux-parametron using 4JL gate"
H. Takayama, “A random-access-memory cell using quantum flux parametron with three control lines”
Y. Xing, “Design and demonstration of power dividers for adiabatic-quantum-flux-parametron logic”

T. Matsushima, “Proposal of analog-digital converter using adiabatic quantum flux parametron”

Y. Okuma, “Reduction of circuit area of AQFP 16-bit multiplexer”

M. Nozoe, “Energy evaluation of the feedback latch using majority gate”

K. Arai, “Design inverter using rf-SQUID and derive an equation of current ratio α”

T. Yamae, "Design of a full adder using the reversible QFP gates"

T. Tamura , “Evaluation of energy consumption for QFPL”

T. Tnaka, “Optimal placement for AQFP IC by using genetic algorithm”